Amendments to the Claims:

The listing of claims will replace all prior versions and listing of claims in the application:

Listing of claims:

1. (Cancelled)

2. (Currently amended) In an integrated circuit (IC) having ~~at least one~~ faults to be tested by fault simulation using ~~at least one~~ a test of a plurality of tests, each ~~of said~~ tests of the plurality of tests including ~~at least one~~ an input test vector, a method for improving the efficiency of the fault simulation comprising ~~the steps of~~:

a) performing a good machine simulation on the ~~said~~ IC with the ~~said at least one~~ test to obtain values of each internal node of the ~~said~~ IC;

b) based on the ~~said~~ good machine simulation, identifying the faults to be ~~in said IC that are potentially~~ tested by the ~~said at least one~~ test;

c) with ~~said at least one~~ the test, performing ~~a~~ the fault simulation on ~~said~~ the faults to be tested ~~that were identified as potentially tested~~; and

d) repeating ~~steps~~ a) through c) for ~~each of said at least one~~ additional tests of the plurality of tests;

wherein ~~step~~ b) further comprises

backtracing from a failing output,

eliminating from the fault simulation any unrelated faults from the faults to be tested that have no structural connection to the failing output, and

eliminating from the fault simulation any duplicate faults from the faults to be tested that are duplicate faults. ~~each observable node, said backtrace through each of said internal nodes being based on said good machine simulation and being limited to paths along which a faulty value has a possibility of propagating to said observable node.~~

3. (Cancelled)

4. (Cancelled)

5. (Cancelled)

6. (Currently amended) The method as recited in claim 2, wherein ~~the~~ observed results of ~~said~~ the test further limit ~~the~~ a number of faults requiring processing by ~~said~~ the fault simulation by starting ~~said~~ the backtraces from only observable nodes wherein ~~a~~ the faults to be tested were ~~was~~ detected.

7. (Cancelled)

8. (Currently amended) In an integrated circuit (IC) having ~~at least one~~ a fault to be tested by fault simulation using ~~at least one~~ a test of a plurality of tests, each test of ~~said~~ the plurality of tests including ~~at least one~~ an input test vector, a method for improving the efficiency of the fault simulation comprising ~~the steps of~~:

a) performing a good machine simulation on ~~said~~ the IC with ~~said at least one~~ the test to obtain values of each internal node of ~~said~~ the IC;

b) based on ~~said~~ the good machine simulation, identifying faults in ~~said~~ the IC that are blocked by ~~said at least one~~ the test from being observed at an observable point of said IC;

c) with ~~said at least one~~ the test, performing ~~a~~ the fault simulation on ~~said~~ the faults that were identified as not being blocked; and

d) repeating ~~steps~~ a) through c) for each test of the plurality of ~~said at least one~~ tests;

wherein ~~step~~ b) further comprises

backtracing from a failing output,

eliminating from the fault simulation any unrelated faults from the faults to be tested that have no structural connection to the failing output, and

eliminating from the fault simulation any duplicate faults from the faults to be tested that are duplicate faults. ~~each observable node, said backtrace through each of said internal nodes being based on said good machine simulation and being limited to paths along which a faulty value has a possibility of propagating to said observable node.~~

9. (Currently amended) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method for improving the efficiency of a fault simulation of an integrated circuit (IC) having ~~at least one~~ a fault to be tested by the fault simulation using ~~at least one~~ test, each of said tests including ~~at least one~~ an input test vector, said method ~~steps~~ comprising:

a) performing a good machine simulation on ~~said~~ the IC with the ~~said at least one~~ test to obtain values of each internal node of ~~said~~ the IC;

b) based on ~~said~~ the good machine simulation, identifying faults in ~~said~~ the IC that are blocked by ~~said at least one~~ the test from being observed at an observable point of said IC;

c) with the ~~said at least one~~ test, performing a fault simulation on ~~said~~ the faults that were identified as not being blocked; and

d) repeating ~~steps~~ a) through c) for each test of the plurality of tests ~~said at least one test~~;

wherein ~~step~~ b) further comprises

backtracing from a failing output,

eliminating from the fault simulation any unrelated faults from the faults to be tested that have no structural connection to the failing output, and

eliminating from the fault simulation any duplicate faults from the faults to be tested that are duplicate faults. ~~each observable node, said backtrace through each of said internal nodes being based on said good machine simulation and being limited to paths along which a faulty value has a possibility of propagating to said observable node.~~

10. (Currently amended) A computer program product comprising: a computer usable medium having computer readable program code means embodied therein for improving the efficiency of a fault simulation of an integrated circuit (IC) having ~~at least one~~ a fault to be tested by ~~said~~ the fault simulation using ~~at least one~~ a test of a plurality of tests, each test of ~~said~~ the plurality of tests including an ~~at least one~~ input test vector, the computer readable program code means in said computer program product comprising:

a) computer readable program code means for causing a computer to perform good machine simulation on ~~said~~ the IC with the ~~said at least one~~ test to obtain values of each internal node of ~~said~~ the IC

b) computer readable program code means for causing the computer to identify faults in ~~said~~ the IC that are blocked by the ~~said at least one~~ test from being observed at an observable point of the ~~said~~ IC, based on the ~~said~~ good machine simulation;

c) computer readable program code means for causing the computer to perform the ~~a~~ fault simulation on ~~said~~ the faults that were identified as not being blocked with the ~~said at least one~~ test; and

d) computer readable program code means for causing the computer to repeat ~~step~~s a) through c) for each ~~of said at least one~~ test of the plurality of tests;

wherein ~~step~~ b) further comprises

computer readable program code means for backtracing from a failing output,

computer readable program code means for eliminating from the fault simulation any unrelated faults from the faults to be tested that have no structural connection to the failing output, and

computer readable program code means for eliminating from the fault simulation any duplicate faults from the faults to be tested that are duplicate faults. ~~each observable node, said backtrace through each of said internal nodes being based on said good machine simulation and being limited to paths along which a faulty value has a possibility of propagating to said observable node.~~

11. (Currently Amended) The method as recited in claim 8, wherein ~~the~~ observed results of the ~~said~~ test further limit ~~the~~ a number of faults requiring processing by the ~~said~~ fault simulation by starting the ~~said~~ backtraces from only observable nodes wherein the ~~a~~ fault was detected.

12. (Currently Amended) The device as recited in claim 9, wherein ~~the~~ observed results of the ~~said~~ test further limit ~~the~~ a number of faults requiring processing by the ~~said~~ fault simulation by starting the ~~said~~ backtraces from only observable nodes wherein the ~~a~~ fault was detected.

13. (Currently Amended) The product as recited in claim 10, wherein ~~the~~ observed results of the ~~said~~ test further limit ~~the~~ a number of faults requiring processing by the ~~said~~ fault simulation by starting the ~~said~~ backtraces from only observable nodes wherein the ~~a~~ fault was detected.